Modulation Method for Single-Phase Six-Switch Five-Level ANPC Inverter

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***Abstract*—The Five-Level Active-Neutral-Point-Clamped (5L-ANPC) inverter is one of the most popular topologies among five-level inverters since it combines the features of Flying-Capacitor (FC) type and Neutral-Point-Clamped (NPC) type inverters and was commercially used for industrial applications. This paper proposes a novel modulation strategy for a Six-Switch 5L-ANPC (6S-5L-ANPC) topology to keep voltages of DC-link capacitors and FC balanced. The equations to calculate the FC capacitance in active and reactive power conditions are also provided. Simulation and experiment have been carried out to demonstrate the effectiveness of the proposed modulation technique.**

Keywords—Multilevel inverter, Active-Neutral-Point-Clamped (ANPC) inverter, Flying-Capacitor (FC), PWM modulation

I. INTRODUCTION

The five-level inverter is a good choice for industrial application because of lower Total Harmonic Distortion (THD), reduced switching stress and hence lower switching losses compared to the three-level inverter [1]. For the conventional Five-Level Neutral-Point-Clamped (5L-NPC) inverter, as shown in Fig. 1 (a), there are three clamping points in the DC-link (P, O and Q). The control strategy to keep voltages of each clamping points is complicated. Additionally, reverse recovery currents from clamping diodes will increase the switching losses of the system. Another conventional five-level inverter topology type is Five-Level Flying-Capacitor (5L-FC) inverter. As shown in Fig. 1 (b), the increased number of capacitors leads to increased volume of the system as well as complex control method to balance the voltages of DC-link capacitors and FCs.

In recent years, hybrid multilevel inverters are receiving more attentions in both academia and industry because they combine the features of many conventional multilevel inverter topologies. As one of the most popular hybrid multilevel inverter topologies, the Five-Level Active-Neutral-Point-Clamped (5L-ANPC) inverter combines the characteristics of NPC type and FC type [2]. As shown in Fig. 2 (a), the 5L-ANPC inverter enables the modularity factor that is lacking in the NPC type inverter by adding the FC power cell to reach higher level without adding series-connected diodes. Additionally, the 5L-ANPC inverter splits the DC-link into two capacitors (C1, C2), so it is simpler to achieve voltage balance between these two capacitors. Due to the reduced cost, volume and control complexity, the 5L-ANPC inverter has gained increasing attention recently and is already commercially used for medium power level industrial applications [3].

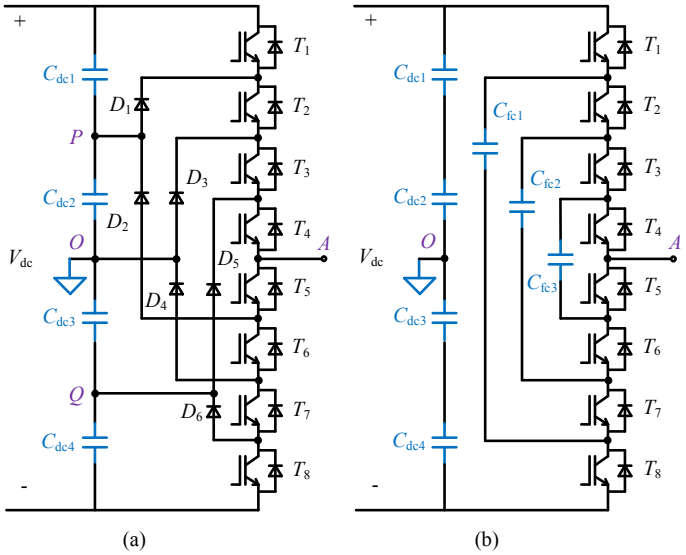

Fig. 1. Conventional five level inverter topologies. (a) 5L-NPC. (b) 5L-FC.

Reference [4] proposed a Six-Switch 5L-ANPC (6S-5L-ANPC) inverter topology to reduce the system cost, as shown in Fig. 2 (b). In contrast to conventional 5L-ANPC inverters, the 6S-5L-ANPC inverter sacrifices some reactive current paths. With special modulation method, the proposed topology has the capability of feeding reactive power into the grid [4]. However, the DC-link capacitor voltage balancing issue is not addressed in its modulation strategy.

To solve the DC-link capacitor voltage balancing problem, many modulation strategies have been presented such as Phase-Shifted Pulse-Width-Modulation (PS-PWM) [5], Selective-Harmonic-Elimination (SHE) PWM [6] and Zero-Sequence voltage injection [7]. However, these methods are suitable for three-phase application. In single-phase application, the DC-link may also experience voltage variation such as Photovoltaic (PV) grid-connected system. It is important to keep DC-link neutral point voltage balanced. Reference [8] designed a modulation method of controlling FC voltage to follow the DC-link capacitor voltage. However, because in each half-cycle only one DC-link capacitor is providing the energy, so it will have a line-frequency voltage disturbance, resulting in the line frequency voltage ripple in FC. Additionally, after each zero crossing point of output current, the FC voltage will change suddenly because its reference voltage is changed. So the complexity of modulation is increased to keep the output current THD. Also,

for 6S-5L-ANPC inverter, under reactive power condition, in reactive power zones, the FC voltage cannot be regulated and is always decreased. This method is not suitable for this application since the FC voltage ripple will be higher. This paper proposes an improved modulation method to keep FC voltage constant in steady state and DC-link voltages balanced.

This paper is organized as follows: Section II describes the operating principles of the 6S-5L-ANPC inverter; Section III discusses the modulation strategy of balancing DC-link capacitor and FC voltages; Section IV provides a design method for the FC capacitance under active and reactive power conditions; Section V and VI give the simulation and experimental results and Section VII draws the conclusion.

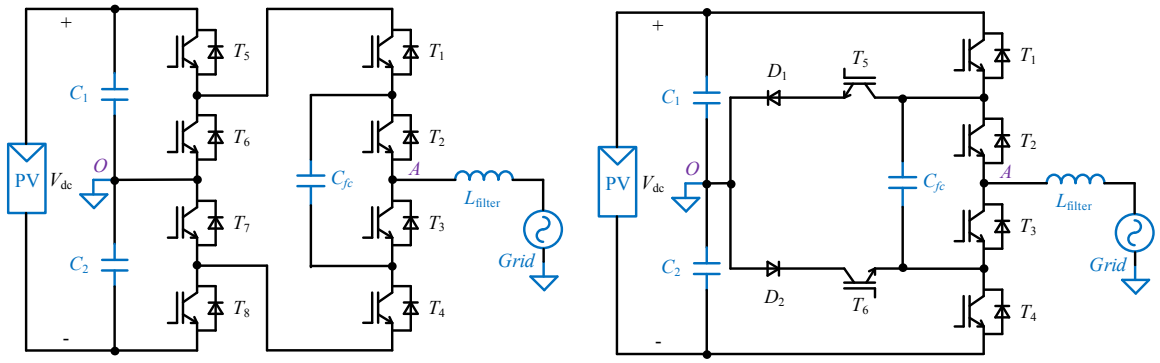

Fig. 2. Configurations of 5L-ANPC inverters. (a) Conventional 5L-ANPC. (b) 6S-5L-ANPC.

II. Operating Principles of 6S-5L-ANPC Inverter

As shown in Fig. 2 (b), the input DC voltage is defined as V_{dc}. The DC-link consists of two series-connected capacitors (C_1, C_2), whose voltages are rated at half of DC voltage ($V_{dc}/2$). A FC (C_{fc}) is required to provide one quarter of DC voltage ($V_{dc}/4$). Therefore, five output voltage levels $+V_{dc}/2$, $+V_{dc}/4$, 0, $-V_{dc}/4$ and $-V_{dc}/2$ (which are defined as +2, +1, 0, -1 and -2 respectively for simplification) are obtained by summing algebraically the DC capacitor and FC voltages.

The 6S-5L-ANPC inverter consists of eight switching states that generate five voltage levels based on capacitor voltages, as shown in Table I. The output current is defined as i_{out}. Fig. 3 shows the specific four switching states in positive grid cycle (states A to D) and current paths (red and green lines show the active and reactive current paths respectively).

TABLE I. Switching States, Output Voltage and Impact on the Voltage of Flying-Capacitor of 6S-5L-ANPC Inverter

No	Switch number						Output voltage level	Flying capacitor C_{fc}	
	T_1	T_2	T_3	T_4	T_5	T_6		$i_{out} > 0$	$i_{out} < 0$
A	1	1	0	0	0	1	+2	--	--
B	1	0	1	0	0	1	+1	Charge	Discharge
C	0	1	0	0	0	1	+1	Discharge	--
D	0	0	1	0	0	1	+0	--	--
E	0	1	0	0	1	0	-0	--	--
F	0	0	1	0	1	0	-1	--	Discharge
G	0	1	0	1	1	0	-1	Discharge	Charge
H	0	0	1	1	1	0	-2	--	--

It is noted that switching states B and C generate +1 level; D and E generate 0 level; F and G to generate -1 level. All four 1 level switching state (B, C, F and G) have impact on FC voltage. In addition, their effect on the FC voltage is opposite to each other. For example, when output current i_{out} is positive, during state B FC is charged while FC is discharged during state C. This leads to the possibility of regulating the FC voltage. The sign of output current i_{out} and FC voltage error are required to decide which redundant switching state to be selected.

Additionally, from Fig. 3, it is observed that the current paths in states C and D are unidirectional. Similarly, the current paths of states E and F are also unidirectional. Therefore, there will be limitations of selecting these four states: when i_{out} is negative, states C and D cannot be used; when i_{out} is positive, states E and F cannot be used. The 6S-5L-ANPC inverter reduces two active switches at the expense of sacrificing its reactive power capability. The maximum reactive power capability can be as low as 0.6 with same FC capacitance and output current THD compared to conventional 5L-ANPC inverters. So it is suitable for PV applications which usually required reactive power capability PF > 0.9.

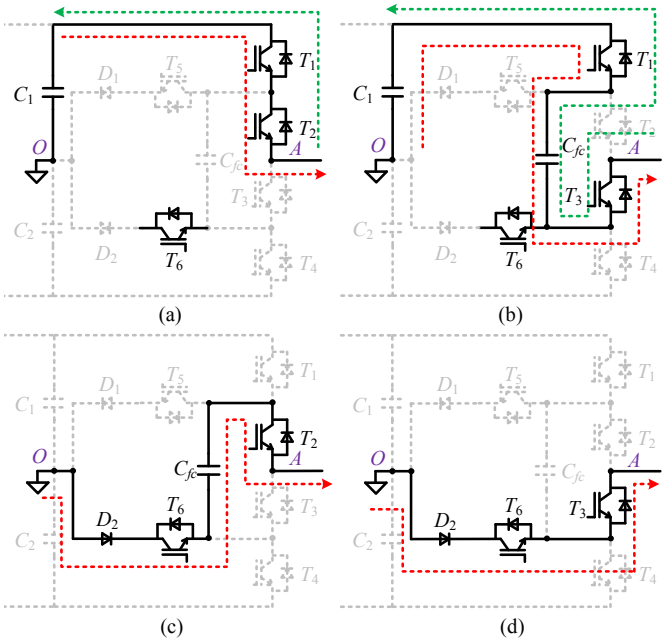

Fig. 3. Switching states of 6S-5L-ANPC inverter in positive grid cycle. (a) State A: +2. (b) State B: +1. (c) State C: +1. (d) State D: +0.

III. Proposed Modulation Strategy

The DC-link capacitor voltage balancing is one problem encountered in single-phase applications, which cannot be solved using three-phase technique such as adding zero-sequence voltage. For 5L-ANPC converters, the output power in positive grid cycle is provided by upper side DC capacitor and FC; similarly, the lower DC capacitor and FC are transferring the energy to the output side during negative grid cycle. If the inverter is controlled to generate symmetrical output current, then the power relationship can be obtained

$$\Delta P_{C1} + \Delta P_{fcp} = \Delta P_{C2} + \Delta P_{fcn} \quad (1)$$

The power transmission relationship is depicted in Fig. 4.

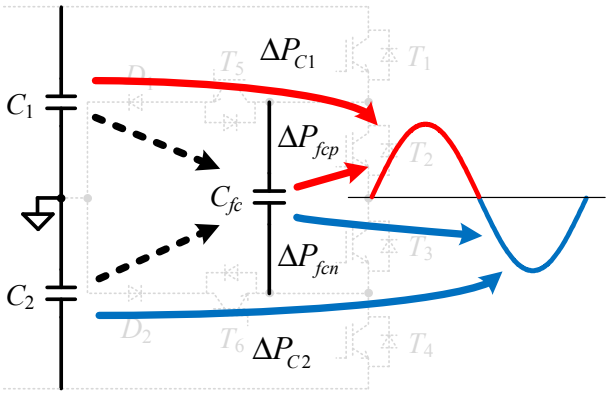

Fig. 4. Relationship of power transmission between DC capacitors, FC and output side during a whole grid cycle

It should be noted that the energy offered by FC (ΔP_{fcp} and ΔP_{fcn}) also comes from DC-link capacitors (the dashed lines). Based on this, the FC voltage can be controlled to regulate the voltages of DC-link capacitors. For example, if V_{C1} is greater than V_{C2}, then in positive grid cycle C_1 can be controlled to transfer more energy to FC and then during negative grid cycle FC is providing more energy to the output side so that C_2 will output less power. Consequently, the voltage difference between two DC-link capacitors will be decreased.

Reference [8] designed a modulation method of controlling FC voltage to follow the DC-link capacitor voltage: the reference FC voltage is designed to follow $V_{C1}/2$ during the positive grid cycle and then follow $V_{C2}/2$ during the negative grid cycle. Fig. 5 shows the simulation waveforms using this method. It is observed that this method will result in the line frequency voltage ripple in FC voltage (the red line in Fig. 5 (a)) since there is a line-frequency voltage disturbance in DC-link capacitors. Additionally, after each zero crossing point of output current, the FC voltage will change suddenly (as can be observed in zoomed waveform in Fig. 5 (a)) because its reference voltage is changed. So the complexity of modulation is increased to ensure the output current THD. Also, for 6S-5L-ANPC inverter, under reactive power condition, in reactive power zones, the FC voltage cannot be regulated and is always decreased. If this method is used for this application, then the FC voltage ripple will be higher. In this paper, an improved modulation method to keep FC voltage constant in steady state and DC-link voltages balanced is proposed.

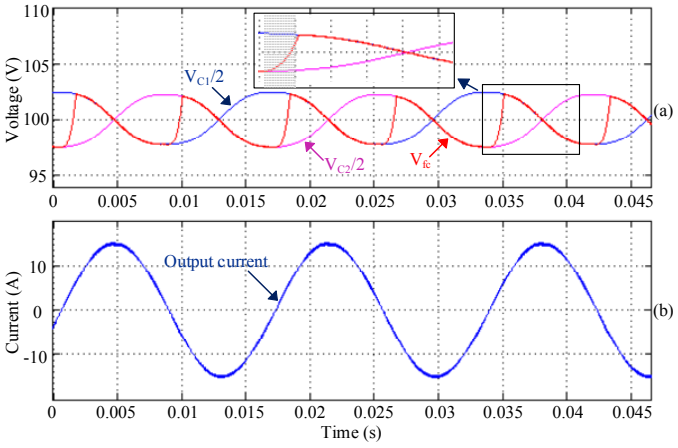

Fig. 5. Simulation waveform using a conventional method. (a) Upper DC-link capacitor voltage $V_{C1}/2$, lower DC-link capacitor voltage $V_{C2}/2$ and FC voltage V_{fc}. (b) Output current.

In positive grid cycle, the output power is applied from the upper DC-link capacitor C_1, so V_{C1} is decreased and V_{C2} is increased; similarly, during negative grid cycle, V_{C2} is decreased to supply the output energy and thus V_{C1} is increased. In balanced condition, during a whole grid cycle or half grid cycle, the average value of both DC-link capacitor voltages V_{C1} and V_{C2} should be balanced at $V_{dc}/2$, as shown in Fig. 6.

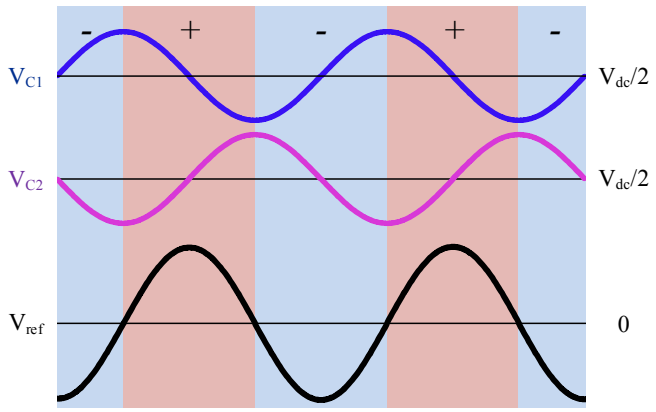

Fig. 6. Voltages of DC-link capacitors under balanced condition

With this motivation, it is possible use average value of DC-link capacitor voltages to determine the FC reference voltage. To achieve this: first, the sampling circuits to sample voltages of two DC-link capacitors are required; during the positive grid cycle, sample the voltage of upper DC-link capacitor voltage V_{C1_n} every switching cycle and then calculate its average value which is defined as V_{C1_av}:

$$V_{C1\_av} = \frac{\sum_{1}^{n} V_{C1\_n}}{n} \quad (2)$$

where n is the number of switching cycles during half grid cycle. This average value will determine the reference FC voltage value $V^*_{fc\_neg}$ in the next negative grid cycle:

$$V^*_{fc\_neg} = \frac{V_{dc}}{4} + k \cdot (\frac{V_{dc}}{2} - V_{C1\_av}) \quad (3)$$

In (2), the proportional control coefficient k multiplied by the DC capacitor voltage error is added to the reference FC voltage. Under balanced condition, the error is closed to zero, so the reference FC voltage should be closed to $V_{dc}/4$.

Similarly, during the negative grid cycle, the voltage of lower DC capacitor voltage V_{C2} is sampled and its average value V_{C2_av} during this half grid period is calculated:

$$V_{C2\_av} = \frac{\sum_{1}^{n} V_{C2\_n}}{n} \tag{4}$$

So the reference FC value $V^*_{fc\_pos}$ in the next positive grid cycle is achieved:

$$V^*_{fc\_pos} = \frac{V_{dc}}{4} + k \cdot (\frac{V_{dc}}{2} - V_{C2\_av}) \tag{5}$$

The diagram of FC reference generator is shown in Fig. 7. The value of coefficient k determines the DC-link capacitor voltage regulation speed. In consideration of small fluctuation of DC neutral point voltage, this value is usually selected to be between 0.5 and 1.

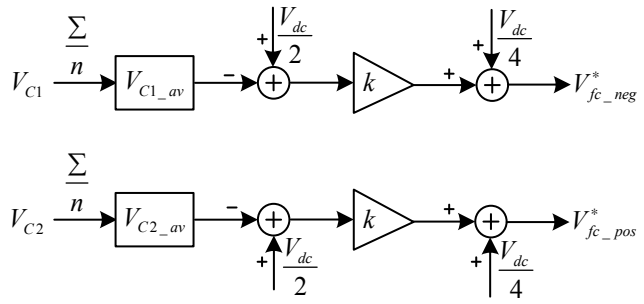

Fig. 7. Diagram of FC reference generator

This averaging modulation technique is effective in achieving balanced FC and DC-link capacitor voltages. Under balanced situation, the FC voltage can be kept constant to $V_{dc}/4$, reducing the FC voltage ripple and hence leading to a simpler modulation. The proposed balancing modulation technique can be applied on any 5L-ANPC topologies.

Under reactive power condition, the modulation of 6S-5L-ANPC converter is different from the conventional 5L-ANPC converter due to the limitation of four unidirectional current flow switching states. Fig. 8 gives the modulation of 6S-5L-ANPC converter under reactive power condition. The power factor (PF) is defined as $cos\ \varphi$. During a complete grid cycle, four operating zones can be identified based on the polarities of the output current and grid voltage: Z1 and Z3 are reactive power zones; Z2 and Z4 are active power zones. In active power zones (Z2, Z4), selection of switching states is the same as conventional 5L-ANPC inverters. The redundant 1 level switching states (B, C) and (F, G) can be used to generate 1 level output and balance the FC voltage. However, in reactive power zones (Z1, Z3), since the inverter output current and voltage are in opposite directions, so the unidirectional current flow switching states C and F cannot be used and hence the FC voltage cannot be regulated, and from analysis it is always decreasing in these regions.

For 6S-5L-ANPC inverter, to balance the DC-link capacitors and FC under reactive power condition, the FC voltage in active power zones (Z2, Z4) is controlled to follow the reference value according to (3) and (5). When power factor is low, the region where FC voltage can be regulated is getting smaller and the FC voltage drop will be higher. In order to keep voltages of each capacitor balanced, a reasonable value of FC capacitance should be selected, which will be discussed in the next section.

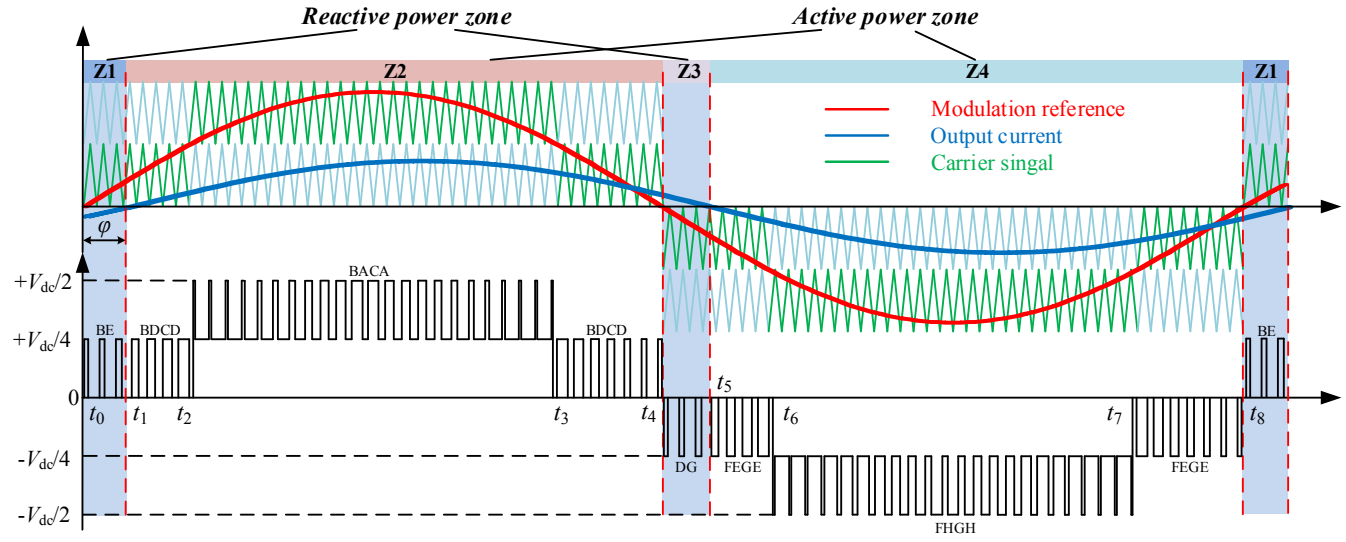

Fig. 8. Modulation of 6S-5L-ANPC inverter under reactive power condition

IV. Flying Capacitor Design

The role of FC in 6S-5L-ANPC inverter is to provide ±1 output voltage levels. In addition to the modulation method which keeps the FC voltage balanced, selection of FC capacitance which limits its voltage ripple is of equal importance to achieve a stable output voltage level. This section gives the parameter design of FC under unity power factor condition and reactive power operating condition.

A. Unity Power Factor Condition

Under unity power factor condition, the FC design is decided by its voltage ripple. Here, the charging time is used to calculate the FC voltage ripple. The modulation index M is assumed to be greater than 0.5 in consideration of high voltage utilization. Fig. 9 gives modulation of 6S-5L-ANPC during positive grid cycle. +2, +1C, +1D and 0 in Fig. 9 represent +2, +1 charging, +1 discharging and 0 output levels respectively.

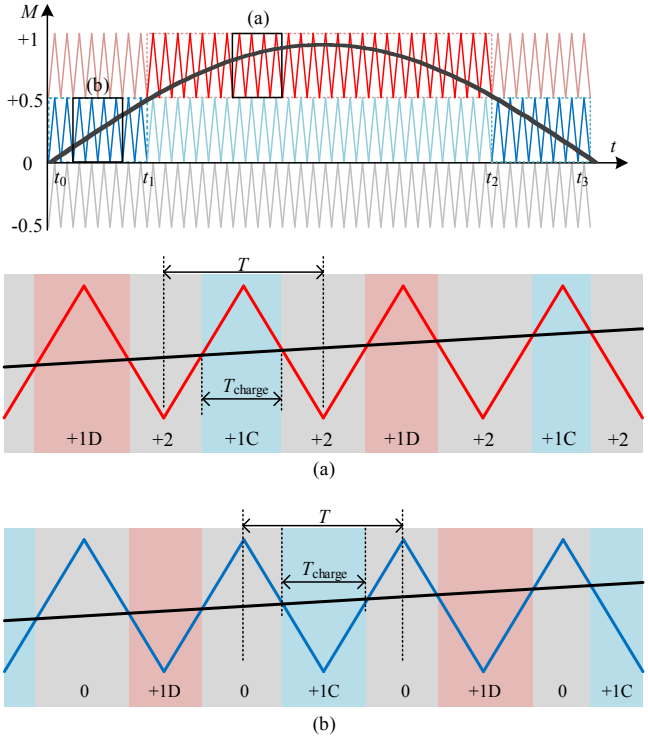

Fig. 9. 6S-5L-ANPC modulation in positive grid cycle. (a) M · sinθ ≥ 0.5. (b) M · sinθ ≤ 0.5.

From Fig. 9, it is obtained that the charging time of FC (T_{charge}) during one switching cycle (T_S) can be written as

$$\begin{cases} T_{charge} = \dfrac{2M \cdot \sin\theta}{f_S} & (M \cdot \sin\theta \le \dfrac{1}{2}) \\ T_{charge} = \dfrac{2(1 - M \cdot \sin\theta)}{f_S} & (M \cdot \sin\theta \ge \dfrac{1}{2}) \end{cases} \tag{6}$$

where f_S is the switching frequency, θ is the reference phase angle. From (6), it is obtained that when $M{\cdot}sin\theta \le 0.5$, the FC charging time function is increasing function; when $M{\cdot}sin\theta \ge 0.5$, it is monotone decreasing function; and it reaches its peak value which is T_S when $M{\cdot}sin\theta = 0.5$.

During the FC charging time T_{charge}, the FC voltage variation ΔV_{fc} can be calculated using

$$\Delta V_{fc} = \frac{\Delta Q_{fc}}{C_{fc}} = \frac{I_{pk} \sin\theta \cdot T_{charge}}{C_{fc}} \tag{7}$$

where I_{pk} is the peak value of output current. According to (6) and (7), the FC voltage ripple can be written as

$$\begin{cases} \Delta V_{fc} = \dfrac{2I_{pk}}{C_{fc} f_S} \cdot M \cdot \sin^2\theta & (M \cdot \sin\theta \le \dfrac{1}{2}) \\ \Delta V_{fc} = \dfrac{2I_{pk}}{C_{fc} f_S} \cdot (-M \cdot \sin^2\theta + \sin\theta) & (M \cdot \sin\theta \ge \dfrac{1}{2}) \end{cases} \tag{8}$$

The FC voltage ripple reaches its peak when $sin\theta = 1/(2M)$. Therefore, the capacitance of FC can be calculated as follows

$$C_{fc} = \frac{I_{pk}}{2\Delta V_{fc} f_S M} \tag{9}$$

B. Reactive Power Condition

For 6S-5L-ANPC inverter under reactive power operation, due to the limitation of redundant switching states selection, the FC voltage cannot be regulated in reactive power zone. According to the analysis earlier, it is observed that FC is continuously discharged in reactive power region. Thus the selected FC capacitance value should be large enough to keep the continuous voltage drop within an acceptable range (e.g. 5% of reference FC voltage). For PV application, the system power factor is usually greater than 0.9 ($cos\varphi$ > 0.9). Thus FC capacitance design is discussed under this condition. Due to the symmetry, the FC voltage drop in reactive power zone Z1 is the same as Z3, thus the FC voltage drop in Z1 is chosen for calculation. Fig. 10 gives reactive power modulation of 6S-5L-ANPC inverter during positive grid cycle.

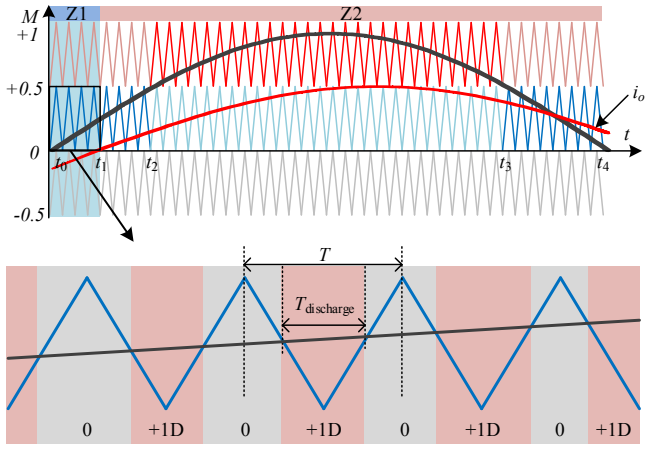

Fig. 10. 6S-5L-ANPC modulation in positive grid cycle under reactive power operating condition.

From Fig. 10, it is observed that in Z1, the output voltage varies between +1 (state B) and 0 (state E). The discharging time of FC ($T_{discharge}$) during one switching cycle is given by

$$T_{discharge} = \frac{2M \sin\theta}{f_S} \tag{10}$$

During each discharging period, the electric charge variation of FC ΔQ_{fc} is calculated according to

$$\Delta Q_{fc} = i \cdot T_{discharge} = \frac{2MI_{pk} \sin^2\theta}{f_S} \tag{11}$$

To calculate the total electric charge of FC in Zone 1, the number of switching cycles N in Z1 is required, which is given by

$$N = \frac{\varphi}{2\pi} \cdot \frac{f_S}{f_{Line}} \tag{12}$$

where f_{Line} represents line frequency. The relationship of FC capacitance C_{fc}, voltage drop ΔV_{fc} and electric charge ΔQ_{fc} is then obtained

$$C_{fc} = \frac{\sum_{n=1}^{N} \Delta Q_{fc}}{\Delta V_{fc}} = \frac{2MI_{pk}}{\Delta V_{fc} f_S} \cdot \sum_{n=1}^{\frac{\varphi}{2\pi}\cdot\frac{f_S}{f_{Line}}} \sin^2\left(n \cdot \frac{f_{Line}}{f_S} \cdot 2\pi\right) \tag{13}$$

C. *Specific Design*

For a 1KVA PV grid-connected system: the grid voltage is 110VRMS; DC voltage is 400V; switching frequency is 15 KHz; modulation index is calculated to be 0.78; the peak-to-peak FC voltage ripple is restricted within 2% of FC voltage. From the FC value calculation equation (9) in unity power factor condition, the calculated FC capacitance value is 275 µF. And if the system is operating under 0.9 power factor condition, with (13), a 3.6V voltage drop is obtained.

V. Simulation Verification

In order to verify the effectiveness of the proposed modulation strategy as well as the FC capacitance calculation, computer simulation by MATLAB/Simulink has been carried out. According to the specific design in previous section: to limit the voltage ripple within 2% under unity power factor condition, the calculated FC value is 275µF and 330µF is selected. The system parameters are shown in Table II.

TABLE II. System Parameters

Power	1 KVA	**Grid voltage (RMS)**	110 V @ 60 Hz
DC-link voltage	400 V	**Output filter inductor**	1.6 mH
Flying capacitor	330 µF	**Power factor**	0.9 - 1
DC-link capacitor	2000 µF	**Switching frequency**	15 KHz

Fig. 11 shows the waveforms of 6S-5L-ANPC inverter using the conventional DC capacitor voltage balancing technique under unity power factor condition. Fig. 11 (a) shows the inverter bridge voltage. Fig. 11 (b) shows voltages of three capacitors. There is line frequency ripple in the FC voltage. Fig. 11 (c) shows the waveform of output current and grid voltage. Fig. 11 (d) shows the THD spectrum of output current. The measured THD of output current is 1.9%.

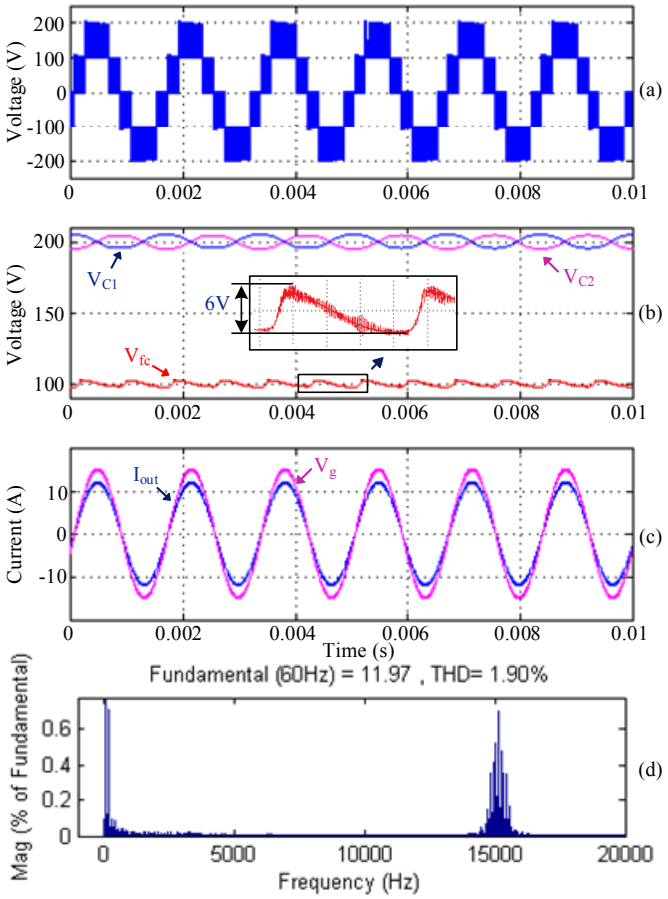

Fig. 11. Simulation results using a conventional balancing modulation technique under unity power factor condition. (a) Bridge voltage. (b) Voltages of upper, lower DC-link capacitors and FC. (c) Output current and grid voltage. (d) THD of output current.

Fig. 12 shows the waveforms of 6S-5L-ANPC inverter using the proposed modulation strategy under unity power factor condition. So in contrast to the conventional method, the difference is that the FC voltage in steady state is a constant value. The measured FC voltage peak-to-peak ripple is 1.8V which verifies the FC capacitance calculation method under unity power factor condition. As shown in Fig. 12 (d), the measured output current THD is decreased to 1.67%, which shows the proposed modulation method has better output performance.

Fig. 13 shows the waveforms under transient state using the proposed method with different proportional coefficient *k*. It is observed that the higher *k* value leads to system entering steady state faster. However, high *k* value may result in oscillation when any DC-link capacitor voltage disturbance occurs. A saturation block can be placed after the FC voltage generator.

Fig. 14 shows the waveforms of 6S-5L-ANPC inverter using the proposed modulation strategy under reactive power condition (PF = 0.9, capacitive). In Fig. 14 (b), it is observed that there are voltage drops in reactive power zones. The measured voltage drop value is 3.8V, which also verifies the FC capacitance calculation method under reactive power condition in previous section. The voltage drop occurs in the region near the zero crossing point. Since the duty cycles of the 1 level

output signal in this region are very small, the FC voltage drop has less impact on the output current THD, which is 1.68% and closed to the output THD under active power condition. Therefore, it can be concluded that under high power factor condition (PF > 0.85), the selection of FC capacitance for 6S-5L-ANPC inverter can be the same as conventional 5L-ANPC inverters without sacrificing the output performance.

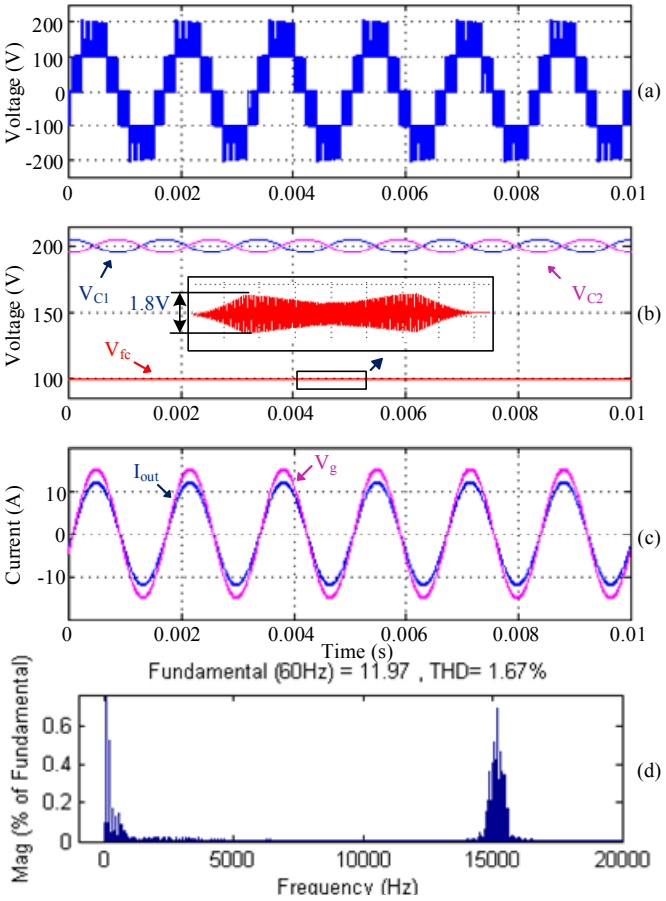

Fig. 12. Simulation results using the proposed balancing modulation technique under unity power factor condition. (a) Bridge voltage. (b) Voltages of upper, lower DC-link capacitors and FC. (c) Output current and grid voltage. (d) THD of output current.

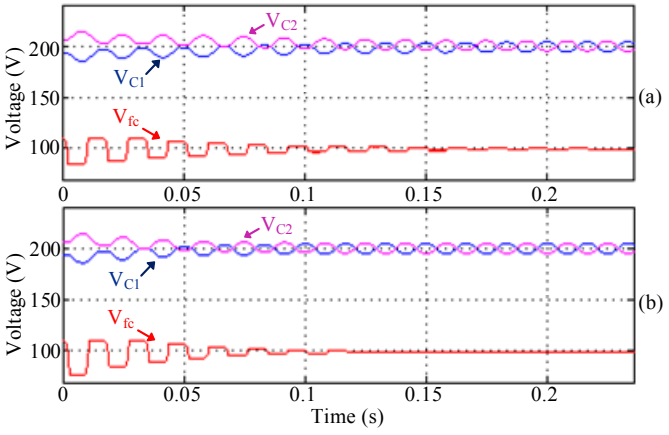

Fig. 13. Waveforms of voltages of three capacitors using the proposed balancing modulation technique with different proportional coefficient *k*. (a) *k*=1. (b) *k*=2.

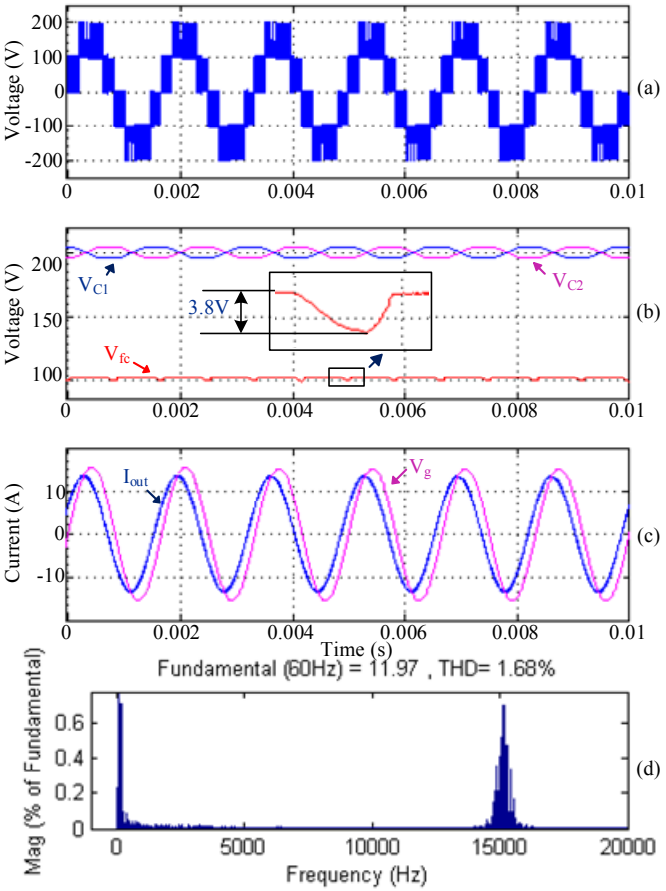

Fig. 14. Simulation results using the proposed balancing modulation technique under reactive power condition (PF = 0.9, capacitive). (a) Bridge voltage. (b) Voltages of upper, lower DC-link capacitors and FC. (c) Output current and grid voltage. (d) THD of output current.

VI. Experiment Verificatoin

A 1KVA single-phase 7S-5L-ANPC inverter grid-connected laboratory prototype is built. The experimental parameters are identical to the ones in simulation section. Fig. 15 shows the waveforms using conventional modulation method under unity power factor condition. The measured output THD is 1.95%.

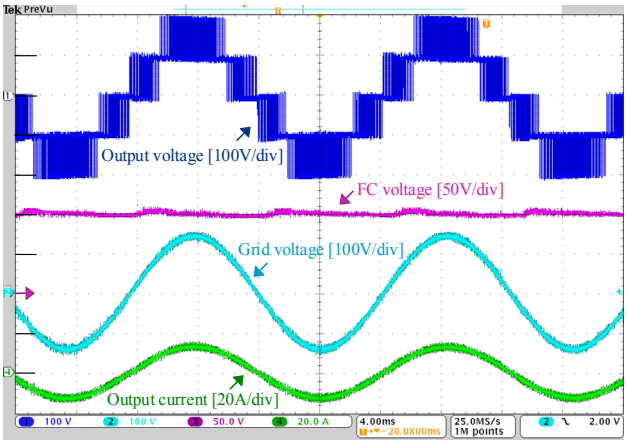

Fig. 15. Experimental results using the conventional modulation strategy under unity power factor condition: output voltage, FC voltage, grid voltage and output current

Fig. 16 and Fig. 17 shows the experimental waveforms using the proposed modulation method under unity power factor condition. The measured THD of output current is 1.7%, which is very closed to the simulation results. Two DC-link capacitor voltages are balanced with a 12V line frequency ripple. The measure FC peak-to-peak ripple is 2V.

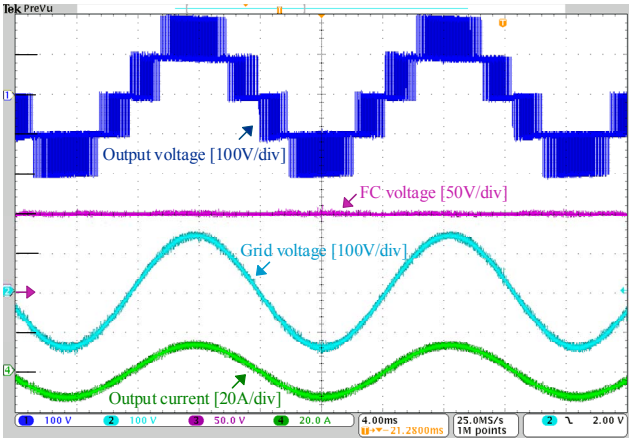

Fig. 16. Experimental results using proposed modulation method (PF = 1): output voltage, FC voltage, grid voltage and output current

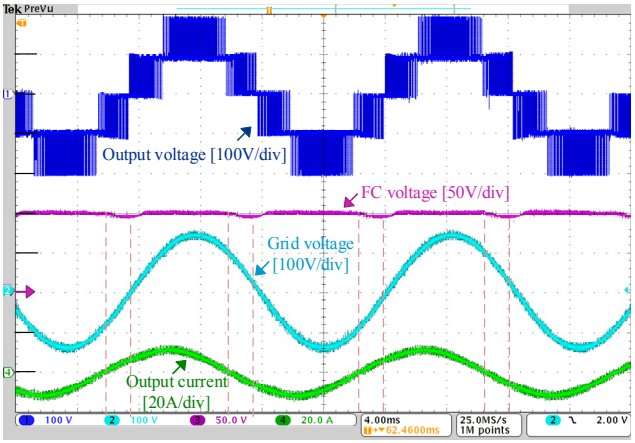

Fig. 18. Experimental results using proposed modulation method (PF = 0.9, capacitive): output voltage, FC voltage, grid voltage and output current

Fig. 18 and Fig. 19 shows the experimental waveforms using the proposed modulation method under reactive power condition. The measured FC voltage drop is 4V. The output current THD is unchanged, which is 1.7%. Two DC-link capacitor voltages are also balanced in this situation whose line frequency ripple is 11.4V.

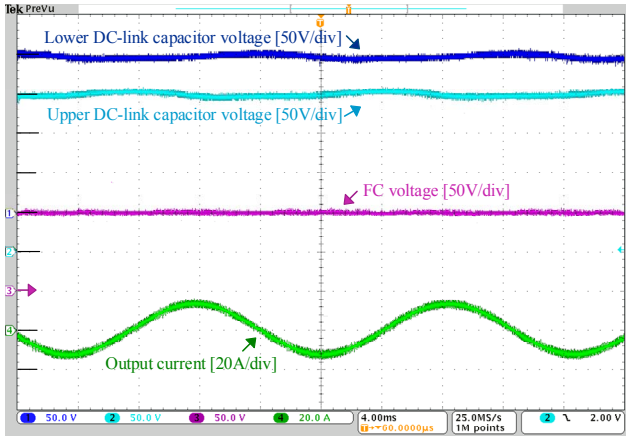

Fig. 17. Experimental results using proposed modulation method (PF = 1): lower and upper side DC-link capacitor voltages, FC voltage and AC current

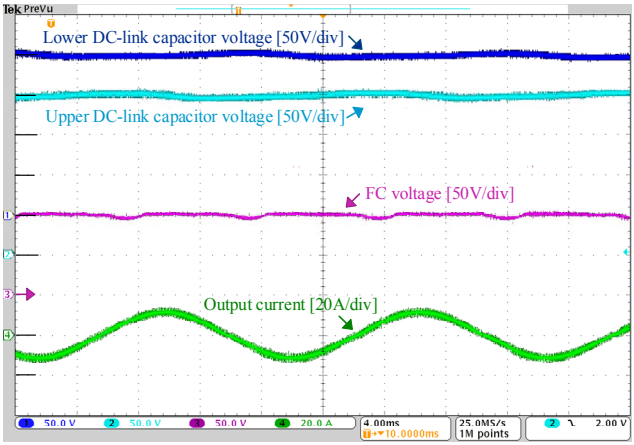

Fig. 19. Experimental results using proposed modulation method (PF = 0.9, capacitive): DC-link capacitor voltages, FC voltage and AC current

VII. Conclusion

In this paper, a novel modulation method to balance DC-link capacitor and FC voltages for 6S-5L-ANPC inverter has been proposed. This averaging modulation technique is effective in achieving balanced FC and DC-link capacitor voltages and leads to a simpler modulation. The proposed balancing modulation technique can be applied on any 5L-ANPC topologies. The equations to calculate the FC capacitance value in active and reactive power conditions are provided. Simulation and experiment have been carried out to demonstrate the reliability of proposed modulation method.

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